

# Polarization reversal and memory effect in anti-ferroelectric materials

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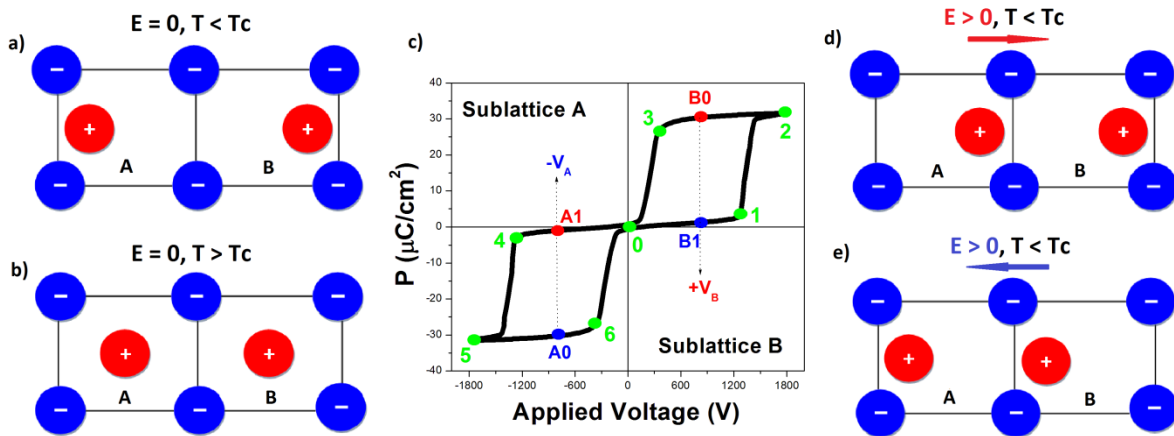
A solid state memory effect is defined as the ability of a material to store information, and it requires at least two switchable memory states that can be addressed by an externally controlled parameter. In this article we present experimental evidence of a memory effect in anti-ferroelectric  $\text{Pb}_{0.99}\text{Nb}_{0.02}[(\text{Zr}_{0.57}\text{Sn}_{0.43})_{0.94}\text{Ti}_{0.06}]_{0.98}\text{O}_3$  polycrystalline ceramic materials. This study indicates that anti-ferroelectrics encode data in their ferroelectric sublattices, resulting in a 4-state memory capable of storing 2 digital bits simultaneously. This result opens up the possibility of realizing non-volatile anti-ferroelectric random access memory, as well as other possible devices and logic applications based on anti-ferroelectric materials.

1. Anti-ferroelectric memory. 2. Antiphase domains. 3. Ferroelectricity. 4. Ferroelectric materials. 5. Electroceramics.

Anti-ferroelectric materials are interesting dielectrics first predicted by Kittel in 1951 using Landau-Devonshire phenomenological theory [1]. The experimental confirmation of the anti-ferroelectric phase in  $\text{PbZrO}_3$  ceramics followed shortly [2,3]. Although there are various models explaining the anti-ferroelectricity, anti-ferroelectric materials remain very much an experimental and theoretical research topic today [4-7]. The motivation of these studies is to advance our understanding of the physics of anti-ferroelectric materials and to facilitate their introduction into technical applications. Indeed, the field induced transition from antipolar to polar dielectric in anti-ferroelectrics gives rise to interesting properties and applications such as high-energy density storage super-capacitors [8-12], electro-caloric solid state cooling [13], piezo-actuation [14], high dielectric permittivities, and many other interesting dielectric phenomena. Here we propose and demonstrate a memory effect in anti-ferroelectric materials. To introduce the concept, we make use of the basic Kittel definition of the anti-ferroelectric as an antipolar crystal consisting essentially of two equally and opposing ferroelectric sublattices. We shall refer to the two ferroelectric phases as Sublattice A and Sublattice B, as shown in figure 1. Under no applied electric field, the anti-ferroelectric has zero polarization due to the self-cancellation of the macroscopic polarizations of the two consisting ferroelectric sublattices. This is well represented in figure 1. a), which shows diagrammatically the zero polarization state and the unit cells of the ferroelectric sublattices A and B, at equilibrium, and under no applied external field. A zero polarization state under no applied electric field is also observed when the system is at a temperature above the Curie transition temperature of the ferroelectric sublattices, as they enter centrosymmetric / paraelectric phases, figure 1.b). The application of a large enough external electric field results in switching of the anti-ferroelectric from antipolar to polar ferroelectric. Therefore, under the influence of an applied electric field, the anti-ferroelectric displays a double hysteresis, with each hysteresis loop representing the response of the induced ferroelectric phase with polarization in the direction of one of the two sublattices. This case is schematically represented in figures 1.d) and e).

Figure 1.c) shows a typical polarization versus electric field / voltage response of an anti-ferroelectric material. As already mentioned, unlike ferroelectrics, which display a single hysteresis loop, the anti-ferroelectric materials display a double hysteresis loop. It is very useful to examine the double hysteresis loop in detail. Let us assign the hysteresis loop occurring at negative applied fields / voltages in figure 1.c) to sublattice A, and the hysteresis

loop occurring at positive voltages as corresponding to sublattice B. Let  $\pm V_s$  be the positive and negative polarization saturation voltages.



**Figure 1.** Schematic diagram of the unit cells of an anti-ferroelectric crystal showing the possible phases depending on the temperature and applied electric field and hysteresis response. a) Anti-ferroelectric phase at zero applied electric field, resulting in fully compensated polarization due to cancellation of A and B sublattice polarizations. b) Para-electric phase of an anti-ferroelectric at  $T > T_c$ , resulting again in zero polarization. c) Polarization versus applied voltage / E field response of a typical anti-ferroelectric material. Key points on the double hysteresis curve are marked, as well as the reversal voltages and quasi-remnant polarization memory states. d) Anti-ferroelectric under the action of a positive E field, showing that sublattice B remains unchanged while A undergoes a hysteresis polarization reversal. e) Anti-ferroelectric under the action of a negative E field, showing the sublattice A unchanged and B undergoing a hysteresis polarization reversal.

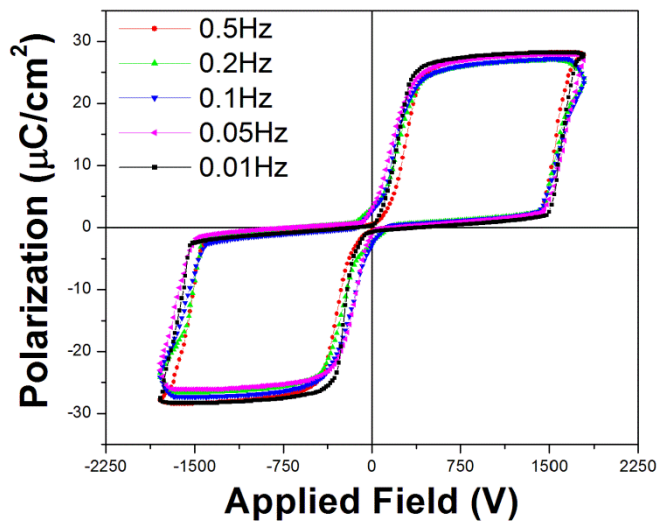
We now introduce the quasi-remnant states of the two sublattices as the remnant polarizations of each sublattice hysteresis loop. They are called quasi-remnant states because, unlike ferroelectric hysteresis where the remnant states occur at zero applied field, here the quasi-remnant states of each sublattice depend on the history of the applied field, but they also occur at a specific applied field, too. We identified  $-V_A$  and  $+V_B$  as the activation fields of the quasi-remnant states for sublattice A and B, respectively (figure 1.c)). In what follows, we will use the convention that A0 and A1 are the digital “0” and “1” memory states corresponding to sublattice A and B0, B1 are the digital “0” and “1” memory states of sublattice B.

If the initial state of the anti-ferroelectric sample is a saturated state at  $+V_s$ , then this corresponds to point 2 on the PE loop, figure 1.c). Lowering the voltage brings the system at point B0, which corresponds to “0” quasi-remnant state of the B ferroelectric sublattice. This state occurs at a positive applied field / voltage,  $+V_B$ , called activation voltage. Continuing to lower the applied voltage, we reach point O at zero applied voltage, where the two sublattices are fully compensated and total polarization is zero. Reversing the applied voltage to negative values, we reach the quasi-remnant state of the second sublattice at point A1, corresponding to the reversal voltage  $-V_A$ . Lowering the voltage further, a negative saturation is reached at point 5 corresponding to  $-V_s$ . Returning to zero voltage, we pass again  $-V_A$  reversal voltage, except that this time a different quasi-remnant polarization state of the sublattice A is observed, A0. When the applied voltage is zero, the system returns back to zero polarization state at point O. Ramping up the positive voltage to  $+V_B$ , the first sublattice reaches another quasi-remnant polarization state corresponding to B1 state. The loop closes back at  $+V_s$ , point 2 on figure 1.c). Points 1, 3, 4 and 6 represent the critical fields of the sublattice reversal, similarly to the coercive fields in an ordinary ferroelectric hysteresis loop.

As shown in figure 1.c), and discussed above, there are four possible quasi-remnant memory states, two for each ferroelectric sublattice. In order to utilize these memory states, the data write operation is accomplished by the simple application of  $\pm V_s$ . However, because of the hysteresis properties of the anti-ferroelectric,  $+V_s$  “write” operation results in encoding a memory state B0 in sublattice B, and a memory state A1 in sublattice A. Similarly, a negative write field  $-V_s$  results in two additional memory states B1 and A0. It is important to stress that accessing these states requires one of the applied activation voltages  $-V_A$  or  $+V_B$ , as shown in figure 1.c). The “write / read” field permutations protocol of the proposed anti-ferroelectric memory and the corresponding four memory states are tabulated in figure 4.d).

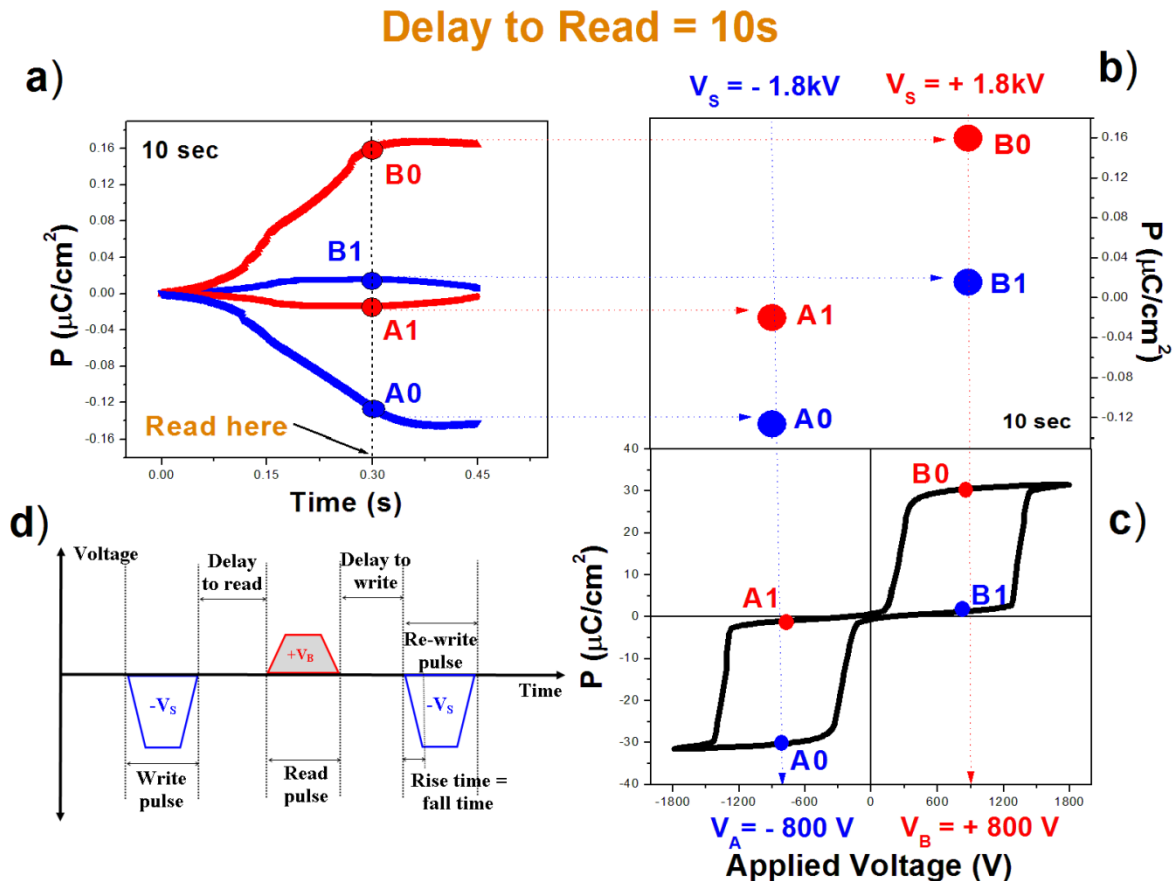
In order to test the proposed memory effect and “write / read” protocol, experimental work was carried out using anti-ferroelectric  $\text{Pb}_{0.99}\text{Nb}_{0.02}[(\text{Zr}_{0.57}\text{Sn}_{0.43})_{1-y}\text{Ti}_y]_{0.98}\text{O}_3$  with  $y = 0.06$  [8]. The code name of the sample is (PNZST 43/100y/2), so for  $y = 0.06$ , our sample is PNZST 43/6/2. To produce the anti-ferroelectric ceramic, powders of  $\text{PbO}$ ,  $\text{ZrO}_2$ ,  $\text{SnO}_2$ ,  $\text{TiO}_2$  and  $\text{Nb}_2\text{O}_5$  with purity levels  $>99.9\%$  were batched with an additional 5 wt.%  $\text{PbO}$  to compensate for  $\text{PbO}$  evaporation during calcination and sintering. Calcination was repeated twice at  $935^\circ\text{C}$  for 4 h for compositional homogeneity. The powder was milled for 7 h in ethanol with zirconia media, dried and pressed. After a final milling of 15 h, 40 g of dried PNZST 43/6/2 powder with acrylic binder was uniaxially pressed at 75 Mpa. Cold isostatic pressing was then applied to the green compact at 400 MPa. After the binder was burnt out at  $450^\circ\text{C}$ , sintering was carried out at  $1325^\circ\text{C}$  for 3 h. To further increase the density of the ceramic, hot isostatic pressing was carried out at  $1150^\circ\text{C}$  and 200 MPa for 2 h in a 20%  $\text{O}_2$ , 80% Ar atmosphere. The final sample used for the present work is a ceramic disk of 10 mm diameter and 500  $\mu\text{m}$  thickness with metallic electrodes applied on each side of the ceramic disk.

Polarization hysteresis loops, as well as memory retention data, were taken using an AiXact Piezo-Test Analyser 2000E. All measurements were performed at room temperature. Hysteresis loops were acquired using a triangular field waveform of 1.8kV amplitude with a pre-polarization pulse applied first. The switching current range was 1 mA for this particular sample and experimental conditions. The waveform frequency was varied from 0.01 to 0.5 Hz and no significant deviations were observed in the double hysteresis loop response, figure 2. All the following measurements were performed at 0.1Hz frequency. From hysteresis measurements we determined the saturation voltage  $V_s = \pm 1.8\text{kV}$ , which corresponds to an electric applied field of 36 kV/cm, and the activation voltage  $V_{A,B} = \pm 800\text{V}$ , equivalent to an electric field of 16 kV/cm. It is important to select the correct “write” voltage so that the ferroelectric sublattices are saturated, but no overall anti-ferroelectric to ferroelectric field induced phase transition is induced.



**Figure 2.** Polarization hysteresis measurements of anti-ferroelectric PNZST 43/6/2 measured at room temperature at various frequencies of the waveform.

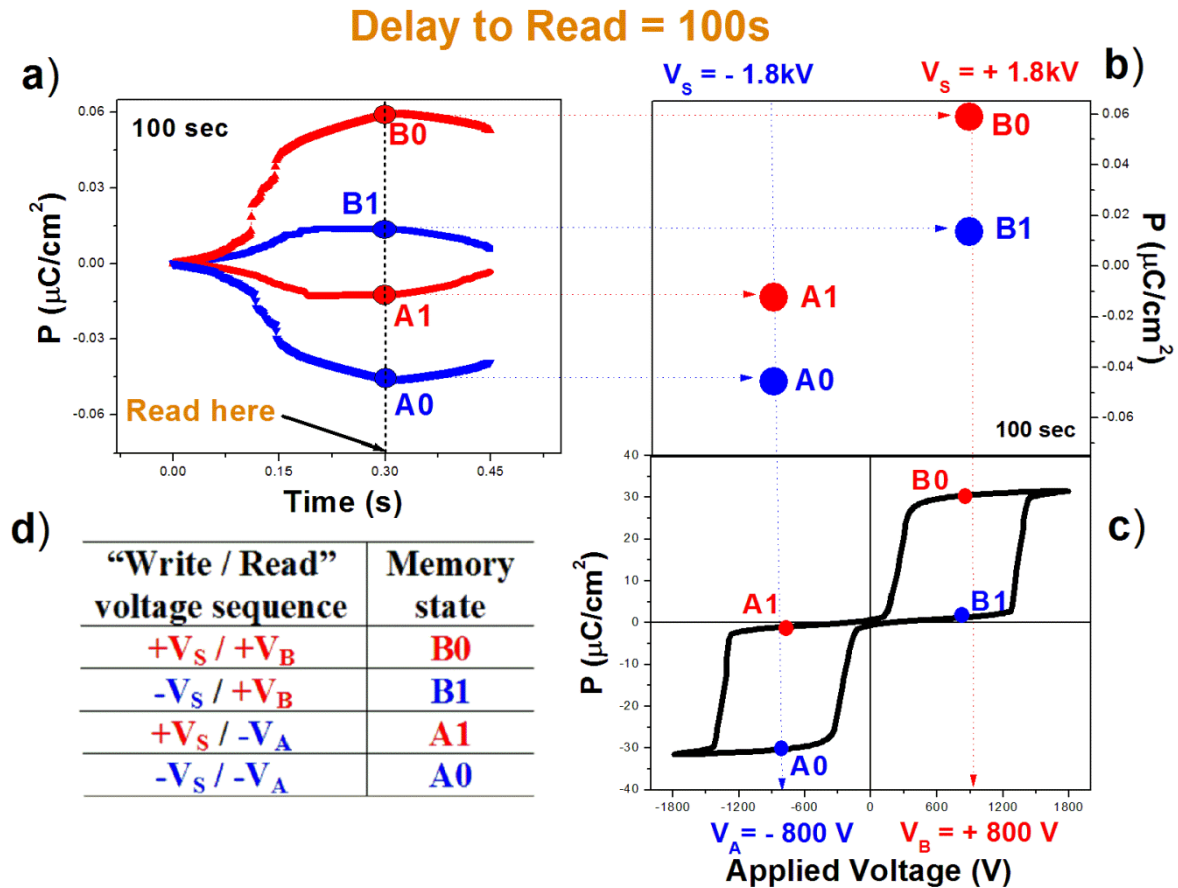
The anti-ferroelectric memory retention experiments were conducted by deploying a measurement test sequence in accordance to the “write / read” protocol described above. The test sequence involved the following steps: i) apply a “write” pulse,  $V_s = +/- 1.8\text{kV}$ ; ii) wait for a time, “delay to read” (DTR); iii) apply a “read” pulse (activation voltage),  $V_{A,B} = +/- 800\text{V}$  and measure the polarization; iv) wait for a time, “delay to write” (DTW); v) apply the “re-write” pulse,  $V_s = +/- 1.8\text{kV}$  accordingly.



**Figure 3.** Anti-ferroelectric PNZST 43/6/2 retention data taken 10 seconds after the “Write” operation. a) Polarization versus time measurement. b) Polarization values of the memory states extracted from the measurement in figure 1.a). c) Anti-ferroelectric PNZST 43/6/2 double hysteresis loop measured at room temperature. The four pseudo-remnant memory states corresponding to a) and b) are clearly marked on the loop. d) Memory test sequence / protocol of “Write / Read” pulses and time delays applied to the experimental testing of the anti-ferroelectric memory effect.

The “write / read” test sequence is diagrammatically represented in figure 3.d). All applied electrical pulses have trapezoidal form, with the total duration of the pulse being equally split in three: rise time, pulse and fall time. The total duration of the “write” pulse was 3s, out of which the rise time is 1s. These relatively long duration pulses were required due to the sample being bulk and requiring large voltages to induce switching. For thinner samples nano-second pulses could easily be deployed. For the “read” pulse we used successfully different durations: 500 $\mu\text{s}$ , 50ms and 150ms, respectively. These are limited by sample response as well as by the measurement system available to us, which has the shortest “read” pulse available of 250 $\mu\text{s}$ . The delay time after read, or the “delay to write” (DTW) time was always fixed to 0.1 $\mu\text{s}$ . This technique was deployed to experimentally “write” and “read” the four memory states of the anti-ferroelectric memory cell. The “delay to read” (DTR) was 10s

and 100s and we successfully demonstrated the memory effect after these durations, which are also limited by the test instrument. The four memory states were addressed using four possible permutations of applied pulses:  $+V_S/+V_B$ ,  $+V_S/-V_A$ ,  $-V_S/-V_A$  and  $-V_S/+V_B$ , respectively, with each permutation corresponding to one possible memory state as tabulated in figure 4.d).



**Figure 4.** Anti-ferroelectric PNZST 43/6/2 retention data taken 10 seconds after the "Write" operation. a) Polarization versus time measurement. b) Polarization values of the memory states extracted from the measurement in figure 1.a). c) Anti-ferroelectric PNZST 43/6/2 double hysteresis loop measured at room temperature. The four pseudo-remnant memory states corresponding to a) and b) are clearly marked on the loop. d) Diagrams of the possible permutations of the "Write / Read" protocol and the corresponding memory states.

Figure 3.c) shows the measured double hysteresis loop corresponding to the PNZST 43/6/2 anti-ferroelectric sample, on which the four pseudo-remnant memory states are clearly marked. Figure 3.a) shows the full measurement of the four memory states after 10 seconds waiting time, determined using the "write / read" test protocol shown in figures 3.d). The measurement is essentially polarization as a function of time, following the "read" field pulse application. The data shown in figure 3 refers to a "read" pulse duration of 150ms, with measurements taken at the end of the pulse,  $t = 300\text{ms}$  and the "delay to read" duration was 10 seconds. A very distinguishable response can be observed with the memory states clearly marked on the polarization versus time curves. Figure 3.b) shows the polarization states corresponding to the four memory states extracted from data in figure 3.a).

The same measurements were repeated by extending the “delay to read” duration to 100 seconds. Figure 4 shows the full measurement of the memory retention after 100 seconds waiting time, using identical parameters as in the previous measurement. Again, a clear distinguishable response can be observed with the memory states clearly marked on the polarization versus time graph, figure 4.a), figure 4.b) and figure 4.c). It is important to notice that we maintained the absolute polarization values on the polarization versus voltage and polarization versus time graphs in figures 3 and 4. This is important because a closer inspection of the data shows that the expected polarization values of the quasi-remanent memory states are much larger than the experimentally measured ones. Figure 3.c) shows that states B0 and A0 should read  $\pm 30 \mu\text{C}/\text{cm}^2$ , while states B1 and A1 should read  $\pm 2 \mu\text{C}/\text{cm}^2$ . Figures 3.a) and b) show that, 10 seconds after the “write” pulse, the extracted polarization memory values are  $\pm 0.16$  and  $\pm 0.02 \mu\text{C}/\text{cm}^2$ , respectively, which are in fact much smaller than expected. When the waiting time was 100 seconds, the “read” values in figures 4.a) and b) are even smaller. This points out to a possible relaxation process, which weakens the retention capacity of the anti-ferroelectric memory. Despite the signal degradation, a measurable 4-state memory effect in anti-ferroelectrics was experimentally demonstrated. Although not clear how allocations of distinct digital “0” and “1” bits to the 4 memory states would work, this study indicates the possibility of utilizing anti-ferroelectric materials for future volatile or non-volatile memory chips [15-17]. Future studies of the memory relaxation process in anti-ferroelectrics are essential to understand the underlying physics and to facilitate their implementation into technological applications. We hope that this work will stimulate such future research of anti-ferroelectric materials and their utilization into volatile or and non-volatile memory chips.

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