Choosing the Most Suitable Analogue Redesign Method for Forward-Type Digital Power Converters

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Abstract

This paper proposes a method to objectively determine the most suitable analogue redesign method for forward type converters under digital voltage mode control. Particular emphasis is placed on determining the method which allows the highest phase margin at the particular switching and crossover frequencies chosen by the designer. It is shown that at high crossover frequencies with respect to switching frequency, controllers designed using backward integration have the largest phase margin; whereas at low crossover frequencies with respect to switching frequency, controllers designed using bilinear integration have the largest phase margins. An algorithm has been developed to determine the frequency of the crossing point. An accurate model of the power stage is used for simulation and experimental results from a Buck converter are collected. The performance of the digital controllers is compared to that of the equivalent analogue controller both in simulation and experiment. Excellent correlation between the simulation and experimental results is presented. This work gives a concrete example to aid academics and engineers to choose a discretisation method with confidence.

Nomenclature

s Laplace operator

z z transform variable

T Sampling period (in seconds)

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f_c	Crossover frequency (in Hz)
ω	Angular frequency (in rad/s)
K_c	Analogue controller gain
K_d	Digital controller gain
V_i	Input voltage (in V)
V_o	Output voltage (in V)
V_r	Ramp voltage (in V)
L	Inductance (in H)
C	Capacitance (in F)
R_L	Load Resistance (in Ω)
R_{esr}	Capacitor ESR (in Ω)
f_s	Switching frequency (in Hz)
ϕ	Phase margin (in $^\circ$)
t_d	Calculation delay (in seconds)
f_o	Frequency of interest (in Hz)
R_{dcr}	DC resistance of inductor (in Ω)
D	Duty
R_{xts}	Secondary transformer winding resistance (in Ω)
R_{xtp}	Primary transformer winding resistance (in Ω)
R_{sw1}	Primary switch resistance (in Ω)
R_{sw2}	Secondary switch resistance, if used (in Ω)
V_{sw1}	Voltage drop across switch 1 (in V)
V_d	Voltage drop across diode or secondary switch (in V)
n	Transformer turns ratio

1 Introduction

Analogue controllers for forward type switched mode power supplies under voltage mode control are typically designed such that the loop frequency response has a crossover frequency of between one twentieth and one tenth of the switching frequency. The crossover frequency and phase margin are related to the settling time and overshoot respectively [1]. The higher the crossover frequency relative to the switching frequency, the faster the settling time of the output voltage. The larger the phase margin the smaller the overshoot. Digital controllers are subject to phase erosion due to the inherent sampling, calculation, and reconstruction delays. Because of this phase erosion a small change in the crossover frequency can have a large detrimental effect on the phase margin, therefore the crossover frequency is commonly restricted to one twentieth of the switching frequency. It is desirable both to increase the crossover frequency and to have a high phase margin for stability and so that the transient response of the digitally controlled system is closer to the transient response of the analogue system.

Analogue redesign and direct digital design control strategies have been used in academia for power supply controller design for many years [2, 3, 4, 5] and have well known relative strengths and weaknesses [6, 7, 8, 9]. The traditional heuristic method of designing analogue controllers lends itself to analogue redesign as the tried and tested stability criteria can be applied. A range of direct digital design methods exist [10, 11, 12, 13, 14, 15] however as the resulting controllers cannot be related back to the stability criteria so easily this paper concentrates on the methods that could be most easily adopted in industry.

Analogue redesign can utilise the same analogue design methods in the frequency domain that have had 30 years of field trials [7, 13]. The same tried and tested stability analysis can be applied and this familiarity gives power engineers confidence in the design of the digital controller by analogue redesign.

Some limited studies have been presented comparing different analogue redesign methods for application to power electronics controllers and it is unusual to find a frequency domain comparison of the analogue redesign methods in the literature. A statement of which discretisation methods may be suitable for both Proportional-Integral (PI) and Proportional-Integral-Differential (PID) controller structures is given in [16] but this is not justified either analytically or experimentally. Some comparative simulationations for the PI and PID controllers are presented in [17, 18] although [17] does not compare the results to those of the analogue controller and neither of these papers give experimental results to verify the simulations. More recently a comparison of the analogue redesign methods has been made for two resonant controllers [19]; this research presents a comparison of the simulated frequency responses for the different discretisation methods and shows that no one discretisation method is favourable for all controllers. Not all discretisation methods are suitable for controller discretisation; Zero Order Hold (ZOH) effects are normally accounted for within the power stage rather than the controller [1]. In the case of [19], the use of the ZOH methods affects the validity of some of the conclusions.

Because of the lack of comprehensive comparisons for the different controller structures, most designers use an approximation method without any consideration of which would be most suitable to meet the performance and robustness specifications [15, 20, 21, 22]. Voltage mode forward-type converters are almost universally controlled using the type-III controller [23] so the work presented here serves to objectively determine which of the analogue redesign methods are most suitable for application to the type-III controller. The sensitivity of the phase margin with respect to the crossover frequency and discretisation method is investigated. A procedure is given that identifies the most suitable discretisation method. This work will allow designers to confidently choose the analogue redesign method which yields the greater phase margin for their application. To clearly demonstrate the process, a 6.6W voltage mode Buck converter is used as a design example throughout the work. The performance of the digital controllers is compared to that of the equivalent analogue controller both in simulation and experiment. An accurate model of the power stage using measured component values gives excellent correlation between simulated and experimental results.

The process of designing a digitally controlled power supply is described in section 2 and followed to introduce the design example in section 3; this design example is used throughout the paper to perform comparisons and analysis of the analogue redesign methods. A comparison of the analogue redesign methods in the frequency domain is made in simulation in section 4. The effects of varying the crossover frequency on the phase margin is simulated in section 5 and includes a procedure to determine the analogue redesign method that will yield the greatest phase margin for a designer's component values, crossover frequency and switching frequency. Finally, detailed experimental results are given, including loop frequency response measurements, in order to verify the simulations in section 6.

2 Digital Power Supply Design

Under digital control a small change in the open loop crossover frequency can have a large detrimental effect on the phase margin so it is prudent to model the power stage accurately. The nominal model [24] has been expanded to include the following parasitic components; capacitor ESR, R_{esr}, inductor DC resistance, R_{dcr}, switch resistances, R_{sw1} and R_{sw2}, voltage drop across switch 1, $V_{sw1} = 0$V, voltage drop across the diode if using a diode or switch 2 if not using a diode, V_d. For forward-type converters under voltage mode control the power stage, derived from first principles, has the general transfer function 1. Note that for non-isolated converters the transformer turns ratio, n, is 1, the primary and secondary transformer winding resistances, R_{xtp} and $Rxts$ are 0, and that for converters using a single switch, the resistance of the second switch, R_{sw2}, is 0.

$$G(s) = \frac{V_i}{V_r} \frac{(1 + sCR_{esr})}{(\frac{s}{\omega_{LC}})^2 + \frac{s}{Q\omega_{LC}} + 1} \tag{1}$$

where

$$\omega_{LC} = \frac{1}{\sqrt{LC(1 + \frac{R_{esr}}{R_L})}}$$

$$R_1 = R_{xts} + R_{sw2} \qquad R_2 = R_{xtp} + R_{sw1} + R_{sw2}$$

$$Q = \frac{\frac{1}{\omega_{LC}}}{\frac{L}{R_L} + C(R_{esr} + (1 + \frac{R_{esr}}{R_L})(R_{dcr} + D(R_1 + R_2 n^2)))}$$

$$D = \frac{V_o + V_d + (\frac{V_o}{R_L})(R_{dcr} + R_{sw2})}{n(V_i - V_{sw1})}$$

For simulation purposes the power stage must be converted to a discrete-time transfer function. As the power stage of the digitally controlled converter is a standard sandwiched plant , as described in [1], it is logical to find the ZOH equivalent of the continuous time power stage 2.

$$G(z) = \left(\frac{z-1}{z}\right) Z\left\{\frac{G(s)}{s}\right\} \tag{2}$$

The ZOH equivalent accounts for the delay in the sampling and reconstruction process and an additional term can be added to account for the calculation delay. The calculation delay is defined as the delay between the sampling instant and the instant when the new control value is applied; it is commonly assumed to be one switching period. Applying 2 to the power stage transfer function results in 3.

$$\begin{aligned} G(z) = {} & nV_i \cdot z^{-t_d} \cdot \\ & \left(\frac{z[1 + \gamma e^{-\alpha T} \sin(\beta T) - e^{-\alpha T} \cos(\beta T)]}{z^2 - z(2e^{-\alpha T} \cos(\beta T)) + e^{-2\alpha T}} \right. \\ & \left. + \frac{e^{-2\alpha T} - \gamma e^{\alpha T} \sin(\beta T) - e^{-\alpha T} \cos(\beta T)}{z^2 - z(2e^{-\alpha T} \cos(\beta T)) + e^{-2\alpha T}} \right) \end{aligned} \tag{3}$$

where

$$\alpha = -\frac{\omega_{LC}}{2Q}$$

$$\beta = \frac{\omega_{LC}}{2} \sqrt{4 - \left(\frac{1}{Q^2}\right)}$$

Table 1: Analogue to digital transforms

Discretisation Method	Transform
Forward integration	$s \rightarrow \frac{z-1}{T}$
Backward integration	$s \rightarrow \frac{z-1}{Tz}$
Bilinear integration	$s \rightarrow \frac{2(z-1)}{T(z+1)}$

$$\gamma = \frac{1}{\beta}(CR_{esr}\omega_{LC}^2 - \alpha)$$

The analogue type-III controller 4 is used for voltage mode control of forward-type converters.

$$C(s) = \frac{K_c(\frac{s}{\omega_{z1}}+1)(\frac{s}{\omega_{z2}}+1)}{s(\frac{s}{\omega_{p1}}+1)(\frac{s}{\omega_{p2}}+1)} \tag{4}$$

The poles and zeros are normally positioned using the traditional heuristic method [24] and the gain is calculated to achieve the desired loop crossover frequency. This analogue controller transforms to the digital controller 5 where the a and b coefficients vary depending on the discretisation method used.

$$C(z) = \frac{K_d(a_0z^3 + a_1z^2 + a_2z + a_3)}{(b_0z^3 + b_1z^2 + b_2z + b_3)} \tag{5}$$

The next step is to apply an analogue redesign method. The best known methods are forward integration, backward integration, bilinear integration, and pole-zero matching [1]. Table 1 shows all of the above transforms apart from pole-zero matching. To apply the desired transform all instances of s are replaced by their z equivalent. Pole-zero matching is applied using the fact that $z = e^{-sT}$. Further information is available in [1].

This process can be followed for any forward type converter under voltage mode control. In order to analyse and perform comparisons of the analogue redesign methods an example converter is required. The next section introduces an design example than will be used throughout the paper for this purpose.

3 Example Buck Converter

3.1 Power Stage

The process in section 2 will be applied to an example Buck converter which will be used throughout the rest of the paper to investigate the performance of the analogue redesign methods at various crossover frequencies. The corresponding physical converter will be used to obtain experimental results. The 6.6W Buck

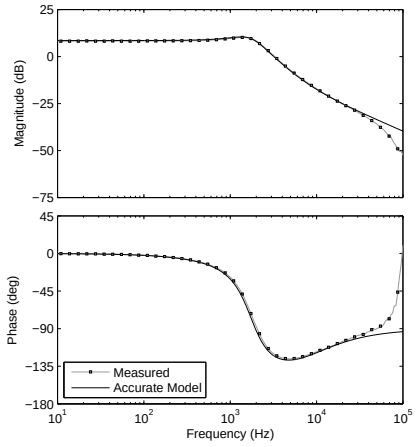

Figure 1: Comparison of measured and simulated analogue power stages (measured using Omecron Lab Bode 100)

converter has the following measured characteristics; capacitance, $C = 500\mu$F, inductance, $L = 15\mu$H, load resistance, $R_L = 1.82\Omega$, $R_{esr} = 45\text{m}\Omega$, $R_{dcr} = 16.5\text{m}\Omega$, $R_{sw1} = 0.3\Omega$ and $V_{sw1} = 0$V. The parasitics were measured using an Omeron Lab Bode 100 network analyser. The reference voltage, V_{ref}, was set to 2.55V and the nominal characteristics of the diode were obtained from the datasheet, $V_d = 0.6$V. As the Buck converter is asynchronous and non-isolated $Rxts = 0$, $Rxtp = 0$, and $n = 1$, and the resistance of switch 2, R_{sw2}, is 0. Substituting these values into the general power stage transfer function results in 6. To obtain the discrete-time power stage transfer function 7, the ramp voltage, V_r, is normalised to 1V and the ZOH equivalent is calculated.

$$G(s) = \frac{12}{V_r} \frac{1.216 \times 10^8 (1 + 2.000 \times 10^{-5} s)}{s^2 + 9529s + 1.216 \times 10^8} \tag{6}$$

$$G(z) = 12 z^{-t_d} \frac{0.013z - 0.010}{z^2 - 1.951z + 0.954} \tag{7}$$

Figure 1 shows that the simulated power stage model and the measured power stage are effectively superimposed up to 30kHz (three twentieths of the switching frequency). The inaccuracy of the model at these high frequencies will not affect the system design or simulation of any stability margins. The power stage model 1 is, therefore, validated.

3.2 Analogue Controller

For a complete comparison the discrete time controllers will be compared to an analogue controller. Analogue control is achieved using the TI UC3825 Pulse

Width Modulation (PWM) controller and V_r was measured as 4.5V. Given the switching frequency the switching period is calculated as 5μs. The desired crossover frequency for the compensated system is 10kHz, $1/20^{\text{th}}$ of the switching frequency. The poles and zeros of the controller are positioned using the traditional heuristic method [24] and the analogue controller gain, K_c, is calculated to achieve the desired loop crossover frequency. The component values required to realise this were modified using those from the E24 resistor series and standard capacitor values. This resulted in the following analogue controller which, when simulated with the Buck power stage, results in a crossover frequency of 7.57kHz with a phase margin of 73.4°.

$$C(s) = \frac{12788(\frac{s}{6667}+1)(\frac{s}{14368}+1)}{s(\frac{s}{51111}+1)(\frac{s}{625000}+1)} \tag{8}$$

To obtain the controller that is to be used for the digital controller design 9, the designed analogue controller 8 can simply be multiplied by the ramp voltage of the analogue PWM controller, in this case 4.5V. This accounts for the normalised value of V_r used in the discrete-time power stage.

$$C(s) = \frac{2841(\frac{s}{6667}+1)(\frac{s}{14368}+1)}{s(\frac{s}{51111}+1)(\frac{s}{625000}+1)} \tag{9}$$

This controller can now be transformed to the z-domain using each of the methods in table 2 and the simulated loop transfer functions will be compared.

4 Comparison of Digital Buck Loop Frequency Responses With Different Discretisation Methods

The analogue controller designed to be discretised 9 was transformed to the z-domain using each of the discretisation methods in table 1; the resulting controllers are shown in table 2. Each of the digital controllers in this table shows a slightly different structure and will therefore have a different frequency response. It is unusual to find a frequency domain comparison of the analogue redesign methods in the literature so this section simulates the loop frequency responses when the power stage of the design example is combined with each of the controllers and compares the results to determine the suitability of each of the methods.

Upon closer inspection of the forward integration controller, a pole is located outside the unit circle resulting in an unstable closed loop system. The forward integration controller will, therefore, no longer be considered and will not be simulated. The remaining controllers described in table 2 were first combined with the discrete-time Buck power stage 7 to obtain the loop transfer functions. The frequency responses of the loop transfer functions were simulated using MATLAB 2012a and v9.3 of the control system toolbox. Figure 2 shows a

Table 2: Discrete time type-III controllers

Discretisation Method	Discrete Controller
Forward integration	$C(z) = \dfrac{4.737z^2 - 8.976z + 4.250}{z^3 + 0.381z^2 - 2.963z + 1.582}$
Backward integration	$C(z) = \dfrac{1.013z^2 - 1.926z + 0.915}{z^3 - 2.039z^2 - 1.232z - 0.193}$
Bilinear integration	$C(z) = \dfrac{0.863z^3 - 0.775z^2 - 0.861z + 0.777}{z^3 - 1.554z^2 + 0.384z + 0.170}$
Pole-Zero matching	$C(z) = \dfrac{1.349z^2 - 2.560z + 1.214}{z^3 - 1.818z^2 + 0.853z - 0.034}$

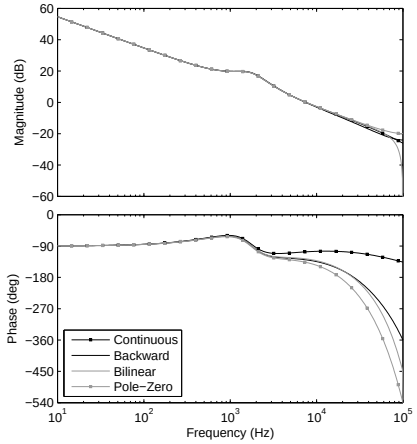

Figure 2: Comparison of loop frequency responses with discretised controllers

comparison of the loop transfer function frequency responses and table 3 gives a summary of the simulated characteristics. The largest deviation, 90Hz, from the analogue crossover frequency is introduced by the backward integration method and the most phase erosion, 30.4°, is introduced by the pole-zero matching method. The bilinear integration method produces the closest phase margin to that of the analogue controller, and by inspection of the Bode diagram, the analogue mangitude locus is most closely followed by the pole-zero matching method.

The phase erosion introduced by discretising the controller using the pole-zero matching method is the largest of the three methods at all frequencies above the resonant frequency. These results suggest that the pole-zero matching method is the least suitable analogue redesign method for the type-III controller and hence it would be better to use either the backward or bilinear integration methods.

Table 3: Comparison of simulated loop frequency responses

Controller Design Method	$\mathbf{f_c}$ (kHz)	ϕ (°)
Analogue	7.57	73.4
Backward integration	7.46	50.6
Bilinear integration	7.58	53.0
Pole-Zero matching	7.58	43.0

This section has shown the differences in the frequency response of each of the discrete time controllers at one crossover frequency as dictated by the analogue controller, 7.57kHz. Interestingly, in figure 2 there is a point where the phase responses of the backward and bilinear controllers cross over. This behaviour suggests that if the designer were to increase the crossover frequency of the design that the method of preference may change; the subject of the next section.

5 Sensitivity in the Phase margin to Changes in Crossover Frequency

The use of the analogue redesign methods results in phase erosion of the loop frequency response. This section investigates how changing the crossover frequency affects the phase margin of the loop frequency responses.

In order to determine the sensitivity in the phase margin to changes in crossover frequency, MATLAB was used to calculate s-domain controllers for crossover frequencies between 1kHz and 30kHz at 1kHz intervals. The switching frequency remained constant at 200kHz, however this is not a limitation and the methods discussed can be applied to any forward-type converter at any switching frequency. Each s-domain controller was converted to the z-domain using the backward integration and bilinear integration methods and combined with the discrete-time Buck power stage 7. The frequency responses of the resulting loop transfer functions were simulated and the phase margins plotted against the designed crossover frequencies (figure 3). These simulations show the two loci crossing at 13.3kHz. Note that the location of this crossing point is not the same as that in figure 2 due to the slight variation in the crossover frequency once the analogue redesign methods have been applied. The implication of this result is that if the designer has chosen a crossover frequency below the crossing point then the bilinear integration method should be used as it produces the highest phase margin, but if the designer has chosen a crossover frequency above the crossing point then the backward integration method should be used. This result is not currently present in the literature but shows that an informed choice of the analogue redesign method can yield the greatest phase margin for the designer's application.

Due to the high order of the discrete time loop transfer functions, it is not possible to derive a simple formula to calculate the crossing point of the two

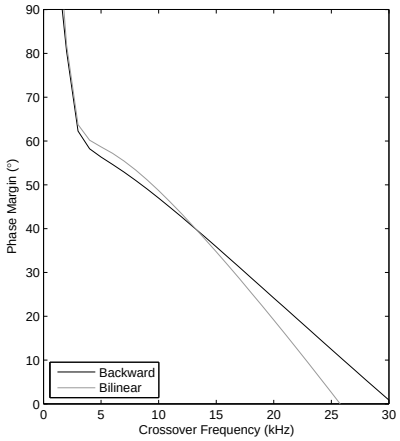

Figure 3: Phase margin against desired crossover frequency for each analogue redesign method

loci in figure 3. Instead a simple algorithm (algorithm 1) has been developed to empirically determine the crossing point. This algorithm is applicable to all forward-type converters at any switching frequency.

When this algorithm is applied to the design example the crossing point is found to be located at a crossover frequency of 13.3kHz, the same as that shown in figure 3. So, in the case of this design example, if the crossover frequency is chosen below 13.3kHz the bilinear integration method yields the highest phase margin, but if the crossover frequency is chosen above 13.3kHz the backward integration method yields the highest phase margin.

6 Experimental Results

To verify the results in sections 4 and 5 hardware experiments were carried out. The analogue controller was implemented using a TI UC3825 high speed PWM controller IC and the digital controllers were implemented using a TI TMS320F2808 microcontroller. Loop frequency responses were captured over the range 10Hz to 100kHz using an Omecron Lab Bode 100 network analyser. Phase margins and crossover frequencies were obtained by inputting the data from the network analyser into MATLAB.

Firstly, one by one the loop frequency resposes of the 6.6W Buck converter with the analogue controller 8 and each of the digital controllers in table 2 were measured. The comparison of the measured results is shown in figure 4 and table 4. The simulation results in figure 2 and the experimental results display similar characteristics at frequencies above the resonant point. The measured crossover frequencies and phase margins almost perfectly match the simulated

Algorithm 1 Determine the crossing point

```
Define switching frequency
Define power stage component values
Generate the forward-type power stage transfer function
Calculate the ZOH equivalent
Generate the analogue controller poles and zeros
Generate a vector of crossover frequencies between the resonant frequency and f_s/2
repeat
  for all Crossover frequencies do
    Calculate gain of analogue controller
    Convert analogue controller to discrete-time using backward and bilinear integration
    Generate discrete-time loop transfer functions
    Find phase margin of loop frequency responses
    Calculate difference between phase margins
    Tabulate the phase margin difference
  end for
  Locate minimum phase margin difference
  if Iteration ≠ MaxIterations then
    Generate new vector of crossover frequencies over smaller range
  end if
until Difference between current and previous minimum phase differences < 0.01
print Crossover frequency with minimum phase margin difference {This is the crossing point}
if Designed crossover frequency ≤ crossing point then
  print Use bilinear integration
else
  print Use backward integration
end if
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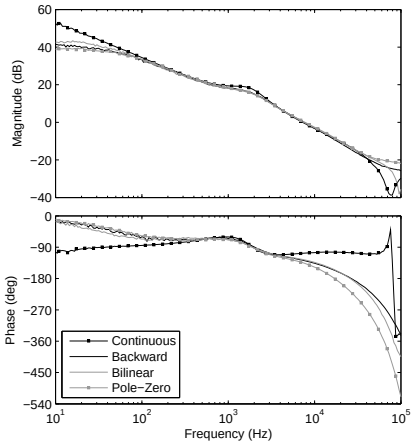

Figure 4: Experimental loop frequency responses measured with Omecron Lab Bode 100

Table 4: Comparison of experimental loop frequency responses

Controller Design Method	$\mathbf{f_c}$ (kHz)	ϕ (°)
Analogue	7.24	72.5
Backward integration	7.59	51.6
Bilinear integration	7.59	53.8
Pole-Zero matching	7.59	44.1

values; the small deviations are due to various fixed point and quantisation effects, measurement resolution, and slight variation in modelled time delays. At frequencies below approximately 100Hz the magnitude plateaus and the phase rises towards 0°; these are due to a measurement error caused by the magnitude of the injected signal at those frequencies being smaller than the analogue to digital converter quantisation levels.

With a designed crossover frequency of 7.57kHz, the bilinear integration controller displays the largest phase margin of the three digitally controlled systems.

Secondly, the effects of varying the crossover frequency were verified at four crossover frequencies (5, 10, 15 and 20kHz). The backward integration and bilinear inegration z-domain controller transfer functions were obtained by applying algorithm 1 at these crossover frequencies. The phase margins of the loop frequency responses of the Buck converter with the controllers designed at these four crossover frequencies were measured and are given in table 5. Figure 5 shows the simulated values overlayed with the experimental values. At 5 and 10kHz, as expected, the measured phase margin of the system when using the bilinear integration controller is larger than that when using the back-

Table 5: Experimental results

Designed $\mathbf{f_c}(\mathbf{kHz})$	Backward $\phi(^\circ)$	Bilinear [1] $\phi(^\circ)$
5.00	54.2	56.8
10.00	46.7	49.9
15.00	37.3	36.1
20.00	24.6	19.2

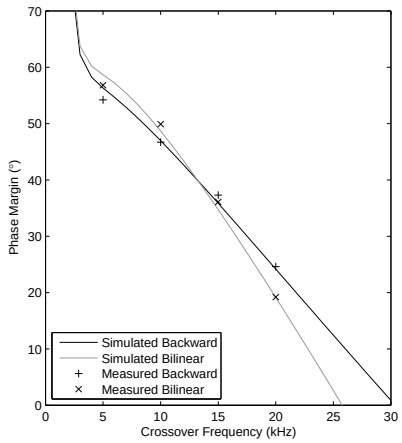

Figure 5: Comparison of simulated and experimental phase margins

ward integration controller, however at 15kHz the measured phase margin of the backward integration controller is larger than that of the bilinear integration controller. This means that experimentally the crossing point is between 10 and 15 kHz, as shown by the simulation. The experimental results confirm that at low crossover frequencies the use of the bilinear integration controller yields the largest phase margin but at high crossover frequencies the use of the backward integration controller yields the largest phase margin.

Both sets of measured results have displayed excellent correlation with the simulations.

In the literature, no directly comparable experimental results have been presented to confirm simulated comparisons of the analogue redesign methods. The experimental results shown in figure 4 and table 4 confirm the simulation results that the pole-zero matching method introduces the largest phase erosion of the analogue redesign methods and is therefore the least suitable method. Of particular interest is the observation that there is a crossing point where, when using crossover frequencies below this point, it is preferable to use bilinear integration to design the controller and, when using crossover frequencies above this point, it is preferable to use backward integration to design the controller.

7 Conclusion

This paper shows, both by simulation and experimental results, that the amount of phase margin erosion varies with the chosen crossover frequency and the analogue redesign method used. Loop transfer functions for a voltage mode Buck converter have been simulated and experimentally obtained to show the relative merits and drawbacks of each method. The forward integration method results in poles outside the unit circle and, therefore, instability. The pole-zero matching method consistently results in the largest phase margin erosion of all of the methods and is therefore also unsuitable. An investigation into the effects of varying the crossover frequency on the phase margin lead from this initial comparison; it was observed that at low crossover frequencies the phase margin obtained by using a bilinear integration method was preferable, but that the gap between the two methods reduces as the crossover frequency is increased until the backward integration method becomes preferable. An algorithm has been developed to determine the crossing point to allow a designer to choose the method that will maximise the phase margin.

A design example of a 6.6W asynchronous Buck converter was shown in this paper. If the analaysis presented is repeated for a specific converter at any switching frequency the best discretisation method for that converter can be chosen given crossover frequency requirements. The same process can be applied to any continuous-time controller structure to determine the approximation method that is most suitable for different controllers.

References

[1] G. F. Franklin, D. J. Powell, and M. L. Workman. *Digital Control of Dynamic Systems*. Addison Wesley Longman Inc., 3rd edition, 1997.

[2] N. Mohan and S. S. Ang. A digital-signal-processor based controller for a switching converter. *International Journal of Electronics*, 77:643–656, 1994.

[3] S. S. Omran, S. M. R. Taha, and M. A. H. Abdul-Karim. Microcomputer-controlled sampling digital power, rms and PF meter. *International Journal of Electronics*, 63:455–461, 1987.

[4] Yuan-Yih Hsu and Wah-Chun Chan. Application of Sliding Modes to Digital Power System Stabilizer Design. *Electric Machines & Power Systems*, 11:171–184, 1986.

[5] Basim A. Hafeth and Majid A. H. Abdul-Karim. Digital power factor meter based on non-linear analogue-to-digital conversion. *International Journal of Electronics*, 58:513–519, 1985.

[6] Yan-Fei Liu, Eric Meyer, and Xiaodong Liu. Recent Developments in Digital Control Strategies for DC/DC Switching Power Converters. *IEEE Transactions on Power Electronics*, 24:2567–2577, 2009.

[7] H. Al-Atrash and I. Batarseh. Digital Controller Design for a Practicing Power Electronics Engineer. In *Proceedings of 2007 IEEE Applied Power Electronics Conference and Exposition*, pages 34–41, Anaheim, CA, USA, 2007. IEEE.

[8] Souvik Chattopadhyay and Somshubhra Das. A Digital Current-Mode Control Technique for DC-DC Converters. *IEEE Transactions on Power Electronics*, 21:1718–1726, 2006.

[9] B.J. Patella, A. Prodic, A. Zirger, and D. Maksimovic. High-frequency digital PWM controller IC for DC-DC converters. *IEEE Transactions on Power Electronics*, 18:438–446, 2003.

[10] Chian-Song Chiu and Chih-Teng Shen. Finite-time control of DCDC buck converters via integral terminal sliding modes. *International Journal of Electronics*, 99:643–655, 2012.

[11] Hebertt Sira-Ramírez, Ciro A. Núñez, and Nancy Visairo. Robust sigmadelta generalised proportional integral observer based control of a buck converter with uncertain loads. *International Journal of Control*, 83:1631–1640, 2010.

[12] Dragan Maksimovic and Regan Zane. Small-signal Discrete-time Modeling of Digitally Controlled DC-DC Converters. In *2006 IEEE Workshops on Computers in Power Electronics*, pages 231–235. IEEE, 2006.

[13] Shamim Choudhury. Digital Control Design and Implementation of a DSP Based High-Frequency DC-DC Switching Power Converter 2 . Digital Control Implementation for DC-DC Converter. In *Proceedings of 2004 Power Electronics Technology Exhibition and Conference*. PET, 2004.

[14] S.M.R. Rafiei, R. Ghazi, R. Asgharian, M. Barakati, and H.A. Toliyat. Robust control of DC/DC PWM converters: a comparison of H_∞, μ, and fuzzy logic based approaches. *Proceedings of 2003 IEEE Conference on Control Applications*, pages 603–608, 2003.

[15] C.E. Lau and M.H. Pong. Comparison of three approaches on DSP based digital controlled 2-wheeler forward converter. In *Proceedings of 1994 IEEE International Conference on Industrial Technology*, pages 164–168. IEEE, 1994.

[16] Aleksander Prodic, Dragan Maksimovic, and Robert W Erickson. Design and Implementation of a Digital PWM Controller for a High-Frequency Switching DC-DC Power Converter IECON ' OI : The 27th Annual Conference of the IEEE Industrial Electronics Society. In *Proc. IEEE Industrial Electronics Society, IECON*, pages 893–898, Denver, CO, 2001. IEEE.

[17] Y Duan and H Jin. Digital controller design for switchmode power converters. *Proceedings of 1999 IEEE Applied Power Electronics Conference Exposition*, 2:967–973, 1999.

[18] T.W. Martin and S.S. Ang. Digital control for switching converters. In *Proceedings of the IEEE International Symposium on Industrial Electronics*, pages 480–484. IEEE, 1995.

[19] Alejandro G Yepes, Francisco D Freijedo, Jesus Doval-Gandoy, Oscar Lopez, Jano Malvar, and Pablo Fernandez-Comesaña. Effects of Discretization Methods on the Performance of Resonant Controllers. *IEEE Transactions on Power Electronics*, 25:1692–1712, 2010.

[20] B. Miao, R. Zane, and D. Maksimovic. Detection of instability and adaptive compensation of digitally controlled switched-mode power supplies. In *Proc. 2005 IEEE Applied Power Electronics Conference and Exposition*, pages 63–69. IEEE, 2005.

[21] M. M. Peretz and Sam Ben-Yaakov. Investigation of Time Domain Design of Digital Controllers for PWM Converters. In *Proc. 2006 IEEE Electrical & Electronics Engineers Convention*, pages 300–304. IEEE, 2006.

[22] A. Prodic and D. Maksimovic. Design of a digital PID regulator based on look-up tables for control of high-frequency DC-DC converters. In *Proc. 2002 IEEE Workshop on Computers in Power Electronics*, pages 18–22. IEEE, 2002.

[23] A. I. Pressman, K. Billings, and T. Morey. *Switching Power Supply Design*. McGraw-Hill, 3rd edition, 2009.

[24] S. Maniktala. *Switching Power Supplies A to Z*. Elsevier, 1st edition, 2006.